

**Edwards & Angell** LLP

101 Federal Street Boston, MA 02110 617.439.4444 fax 617.439.4170  
www.EdwardsAngell.com

**Date :** April 1, 2005**Pages (including cover) :** 5**Sender :**

Name Steven M. Jensen  
Fax 617.439.4170 Phone 617.517.5531  
Email SJensen@EdwardsAngell.com

Re: Our Docket No. 60417 (71987)  
U.S. Serial No. 10/728,304

To :	Fax	Phone
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Docket No. 60417 (71987)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANT: C. Chen et al.

U.S. SERIAL NO.: 10/728,304

EXAMINER: T. Nguyen

FILED: December 3, 2003

GROUP: 2829

FOR: CHIP CARRIER AND METHOD FOR TESTING ELECTRICAL  
PERFORMANCE OF PASSIVE COMPONENT**CERTIFICATE OF FACSIMILE TRANSMISSION**

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By: 

Steven M. Jensen

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**RESPONSE TO OFFICE ACTION**

Applicants are in receipt of the Office Action dated December 1, 2004 of the above-referenced application. A request for a one-month extension of time is submitted herewith. Applicants respond to the Office Action as follows.

Applicants' claimed invention is directed to a chip carrier and a method for testing electrical performance of a passive component. The Applicants' claimed invention is particularly suitable for receiving a passive component such as a resistor or inductor that is serially connected to a conductive trace of a chip carrier.

As recited in claims 1 and 8, a chip carrier according to the Applicants' claimed invention includes a first trace connected with the passive component, the first trace being formed at a predetermined position and having two ends electrically respectively connected to a first bond

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finger on a top surface of the chip carrier, and a first ball pad on a bottom surface of the chip carrier. As recited in claims 1 and 8, the first predetermined position and the first bond finger are located on the same side relative to the passive component.

Also, as recited in claims 1 and 8, a second trace not connected to the passive component is formed at a second predetermined position located on the same surface as the first predetermined position. One end of the second trace is electrically connected to a second ball pad located on the same surface as the first ball pad. Further, the first and second predetermined positions are exposed from a solder mask layer applied on the chip carrier.

Applicants' claimed invention can provide significant benefits. The above-described arrangement enables the exposed first and second predetermined positions to be electrically interconnected by an electrically conductive material to form a short circuit, such that the first and second ball pads on the same surface serve as test points contacted by test heads to perform an electrical performance test.

Claims 1-6, 8, 11-15, and 17 were rejected under 35 USC 102(b) as being anticipated by "Admitted Prior Art" (APA). Claims 7 and 16 were rejected under 35 USC 103(a) as being unpatentable over APA in view of U.S. Patent 6,078,186 to Hembree et al. Claims 9 and 10 were rejected under 35 USC 103(a) as being unpatentable over APA in view of U.S. Patent 5,698,895 to Pedersen et al. These rejections are respectfully traversed.

Referring to FIGS. 7A, 7B, and 8 and the Background of the Invention section of the specification, a passive component 81 (such as a resistor or inductor) is serially connected to a conductive trace 82 of a substrate 80. The conductive trace 82 is electrically connected to both a ball pad 87 on a bottom surface of the substrate, and a bond finger 85 on a top surface of the substrate. The bond finger 85 and ball pad 87 on the top and bottom surfaces of the substrate are electrically connected to the passive component and serve as test points contacted by test probe heads 61 to perform an electrical performance test (see FIG. 8). According to this arrangement, the test probe heads 61 are applied to **different** surfaces.

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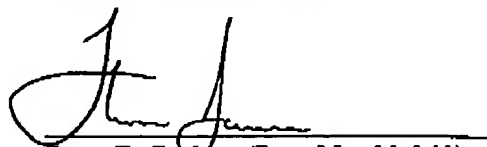
"APA" does not teach or suggest a second trace not connected to the passive component. Also, APA does not teach or suggest first and second predetermined positions formed on the first and second traces, respectively, and exposed from a solder mask layer. Further, APA does not teach or suggest the first predetermined position and the first bond finger located on the same side relative to the passive component. Moreover, APA does not teach or suggest that one end of the second trace is electrically connected to the second ball pad on the bottom surface of the chip carrier.

APA does not teach or suggest the first and second ball pads both located on the bottom surface of the chip carrier to serve as test points, such that test heads can contact the test points located on the same surface to perform the test. Additionally, APA does not teach or suggest electrically conductive material to interconnect the exposed first and second predetermined positions to form a short circuit to perform the test.

For at least the reasons discussed above, the alleged "APA" does not anticipate or otherwise render obvious the Applicants' claimed invention. Therefore, independent claims 1 and 8, and dependent claims 2-7 and 9-17 are patentable over APA.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



Peter F. Conless (Reg. No. 33,860)  
Steven M. Jensen (Reg. No. 42,693)  
EDWARDS & ANGELL, LLP  
P.O. Box 55874  
Boston, MA 02205

Date: April 1, 2005

Phone: (617) 439-4444

Customer No. 21874